

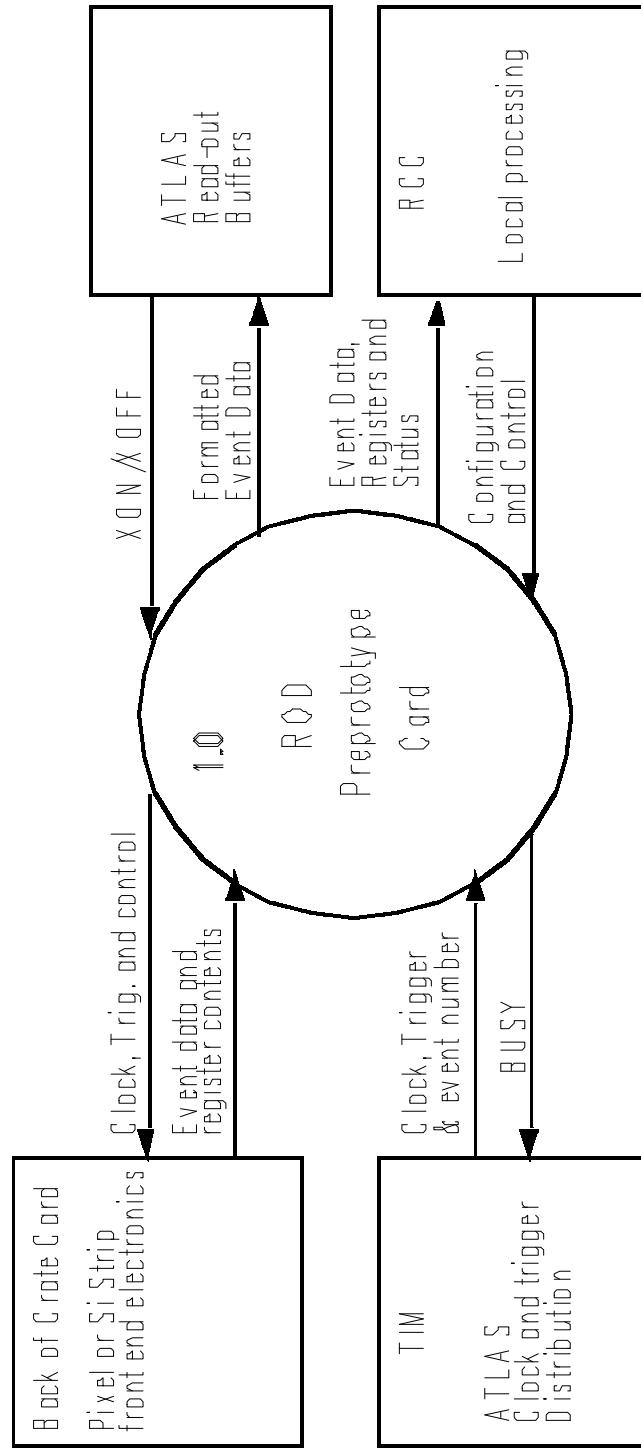
ROD Overview

December 17, 1999

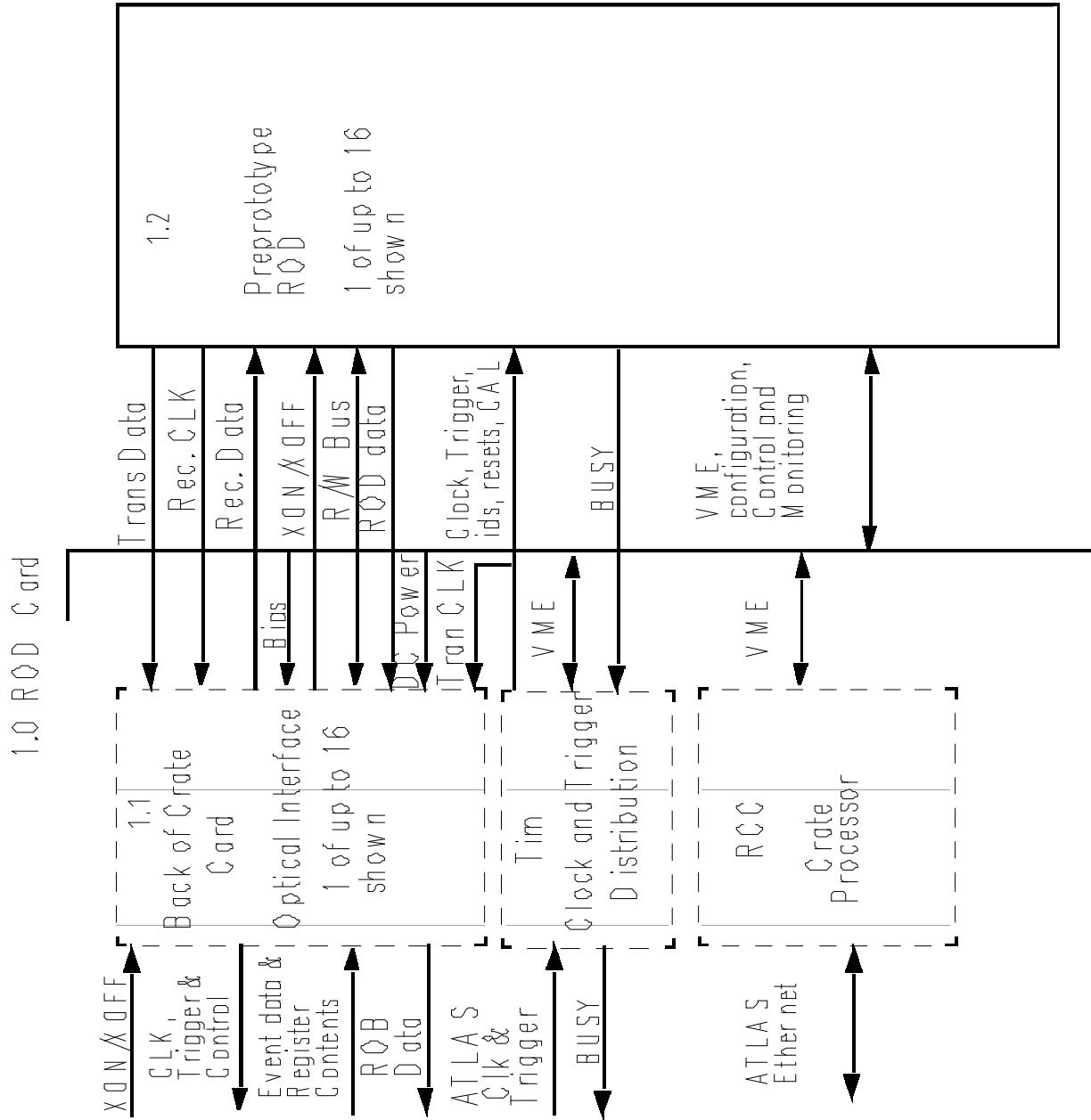
Wisconsin

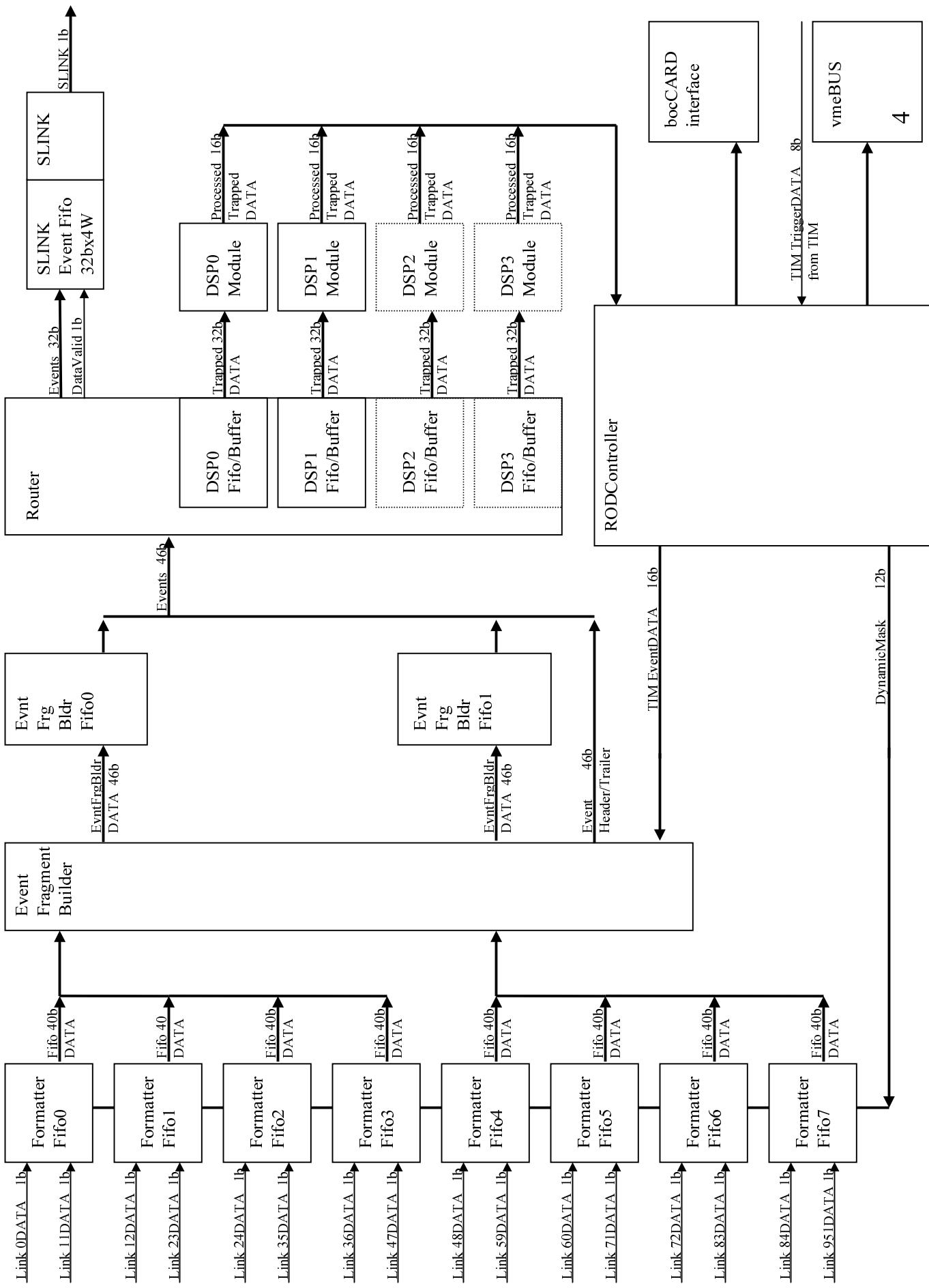
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ROD Overview



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ROD Overview

Changes since the last review

1. The formatter has been changed to reduce the link to link latency from three to one clock tick. The resultant throughput rate is about 60 MHz, dependent on the data volume. The bottle neck is still the s-link.
2. The external FIFO on the formatter have been incorporated in to the FPGA.
3. The utilization of the formatter FPGA is at 64%
4. The dynamic link mask is presented to formatter not the event fragment builder.

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Changes since the last review

5. The number of back end DSPs has been changed from two to four. Only two will be loaded in the cards.
6. Error scaling and diagnostics have been moved to the back end DSP. This has resulted in more extensive error diagnostics.
7. The ROD interfaces have been refined.
8. Simulations have been refined on the pixel and SCT ROD. This has resulted in a clear understanding of the number of RODs.